UNIVERSITY OF CALIFORNIA
Department of Electrical Engineering and Computer Sciences
CS150 Fall 2001

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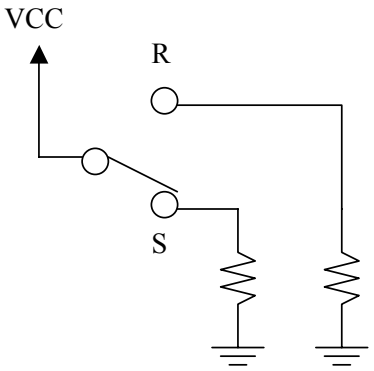
Homework #2

Due: Friday, September 21, 2001

1.

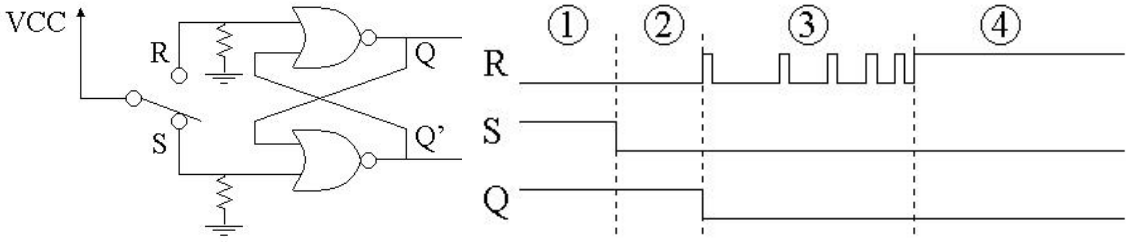
a. The figure shows a diagram of a mechanical switch. The resistors connect the terminals to ground (GND) whenever the switch is not making contact. When the switch makes contact to one terminal, it connects it to VCC. Imagine that you move the switch from the S to the R position. Draw the output waveforms (at R and S) during the transition, identifying the following stages:



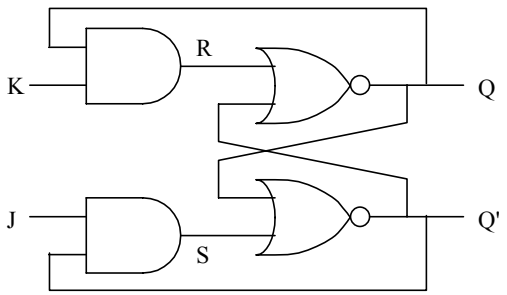
   i. the switch is making contact with the S terminal
   ii. the switch is moving from the S to the R terminal
   iii. the switch touches the R terminal, but bounces 5 times alternating short periods of contact and non-contact
   iv. the switch finally remains steady making contact with terminal R

b. Draw a schematic showing how to connect an R-S flip-flop to eliminate the effects of bouncing. Draw a time diagram showing the outputs of the flip-flop in the case described in a).

Solution

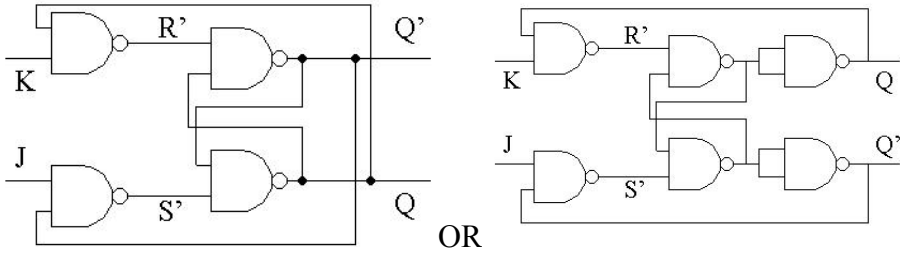


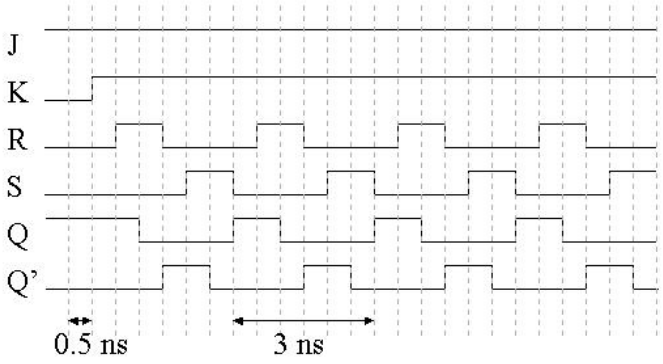
2. The figure below shows a schematic of a J-K flip-flop.



a. Find an equivalent circuit built completely with NAND gates. Indicate clearly the inputs and outputs of the new circuit. (Hint: use De Morgan's law.)
b. Suppose the inputs are (J=1, K=0), and then K goes to 1. Make a time diagram of the transitions on J, K, R, S, Q and Q' after the change on the inputs, assuming all gates have a fix delay equal to .5ns. Which will be the frequency of the oscillations in the output?

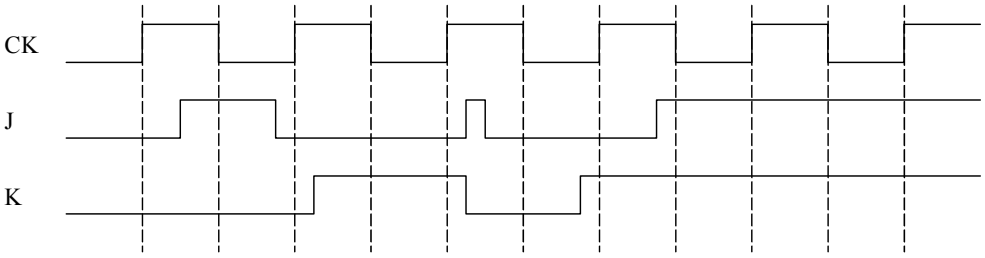
Solution



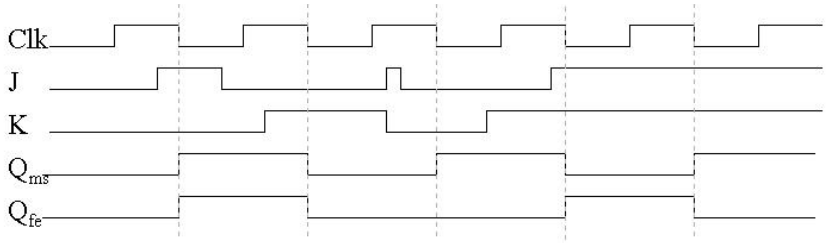


$$F_Q = \frac{1}{T_Q} = \frac{1}{3ns} = 333{,}333{,}333.333\,\text{Hz} = 333\,\tfrac{1}{3}\,\text{MHz}$$

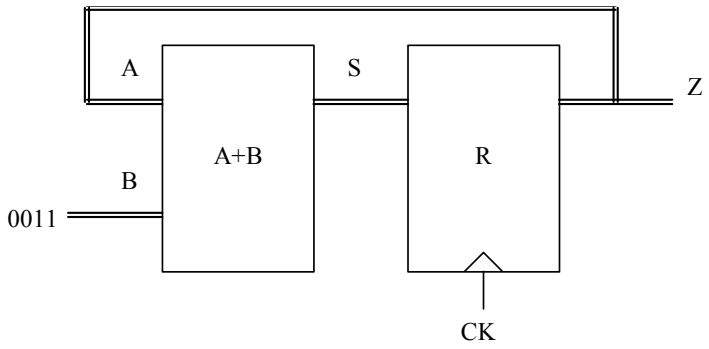
3. Draw the outputs of a master-slave and a falling-edge-clock J-K flip-flops given the inputs in the time diagram (suppose both flip-flops have an initial state Q=0.)



Solution

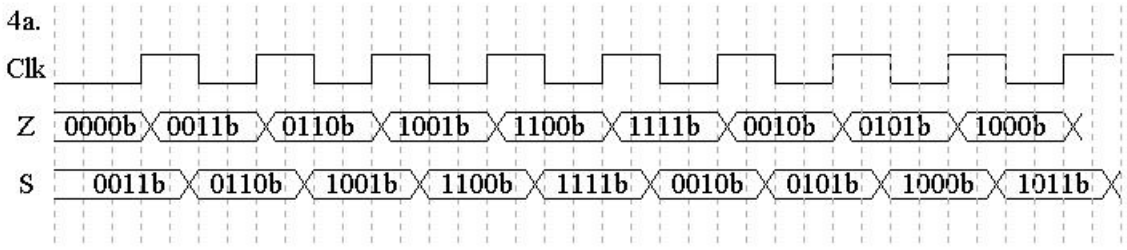


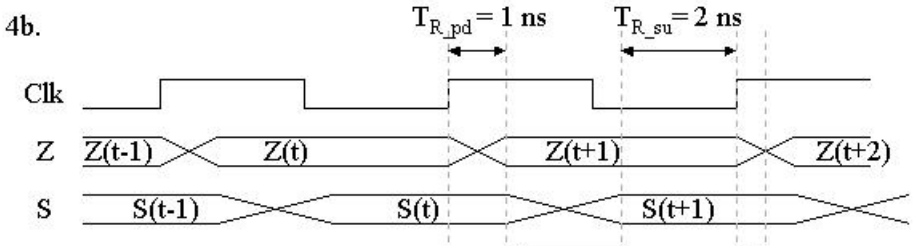
4. We are going to use the 4-bit adder designed in Lab. 1 to construct the circuit in the figure (double traces indicate 4-bit buses). The register R consists of 4 D flip-flops commanded by the same clock signal. The input B of the adder is connected to the value 0011b.



   a. Draw a time diagram indicating the outputs S and Z for 8 clock periods, assuming the register R is initially 0000b.
   b. Given the maximum delay of the adder (td=2ns), and the propagation delay, the set-up and hold times of the D flip-flops (tp=1ns, tsu=2ns, th=.5ns), compute the maximum frequency of the clock signal at which the circuit will work properly.

Solution

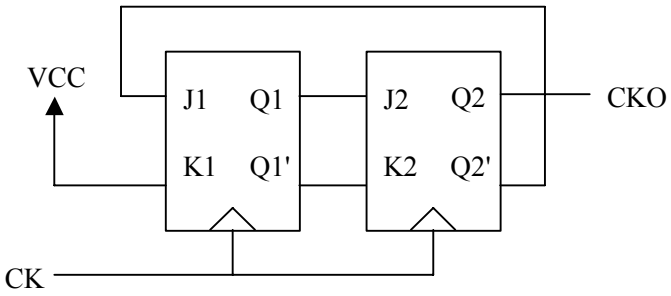




T_{clk} – clock period
T_{R_pd} – register propagation delay
T_{R_su} – register setup time
T_{ff_h} – register hold time
T_{add_pd} – adder propagation delay
F_{clk} – clock frequency

$$F_{clk} = \frac{1}{T_{clk}} = \frac{1}{5ns} = 200000000 \text{ Hz} = 200 \text{ MHz}$$

5. The schematic shows a circuit which is claimed to be a "frequency divider" or a "divider by *N*" circuit. Draw a time diagram of the clock signal and the outputs Q1 and Q2 (CKO) for at least 5 clock periods. Which is the frequency of the output CKO with respect to the clock frequency? What would be the value of *N*?



Solution