Student paper Suggested Area: Displays, Sensors, and MEMS

A high-performance all-inkjetted organic transistor technology

Steven E. Molesa, Steven K. Volkman, David R. Redinger, Alejandro de la Fuente Vornbrock, and Vivek Subramanian

Department of electrical engineering and computer sciences, University of California, Berkeley

We report on the highest performance all-printed transistors reported to date. Using nanoparticle-based printed contact, polymer dielectrics, and a printed pentacene semiconductor, we demonstrate all-inkjetted devices with mobilities > 0.1cm^2/V-s and on-off ratios of ~10^4. These devices represent a significant step towards the realization of low-cost printed electronics.

0-7803-8684-1/04/$20.00 ©2004 IEEE

A high-performance all-inkjetted organic transistor technology

Steven E. Molesa, Steven K. Volkman, David R. Redinger, Alejandro de la Fuente Vornbrock, and Vivek Subramanian
Department of electrical engineering and computer sciences, University of California, Berkeley
144MB Cory Hall, Berkeley, CA 94720-1770, Ph (510) 643-4232, Fax (510) 642-2739, Email: molesas@eecs.berkeley.edu

Abstract: We report on the highest performance all-printed transistors reported to date. Using nanoparticle-based printed contact, polymer dielectrics, and a printed soluble pentacene precursor semiconductor, we demonstrate all-inkjetted devices with mobilities > 0.1cm^2/V-s and on-off ratios as high as 10^4. The performance of these devices is comparable to control devices fabricated on silicon-substrates, and thus, these devices represent a significant step towards the realization of low-cost printed electronics.

Introduction: There is great interest in printing for realizing low-cost electronics. In particular, organic semiconductors are considered a promising means of realizing such systems. In recent years, several organic materials have been used to demonstrate devices with mobilities approaching or exceeding 1cm^2/V-s. Unfortunately, all such devices have been fabricated using either silicon substrates with thermally grown oxides or using vacuum sublimated materials. To achieve the requisite low-cost, it is necessary to achieve such performance levels using printing without the need for silicon substrates or vacuum processing. Till now, the performance of printed devices has lagged substantially, with most reported devices having mobilities <10^{-2}cm^2/V-s, which is too low for most applications.

In this work, we report on all-printed devices with mobilities as high as 0.1-0.2cm^2/V-s and on-off ratios as high as 10^4. The performance achieved in these devices is substantially greater than ever reported before for all-printed devices, and is finally in the performance realm for which potential applications exist for a printed electronics solution.

Experimental Details: The devices herein were fabricated entirely using inkjet printing. However, it should be noted that all the materials used here are not unique to inkjet and should be transferable to high-throughput printing technologies such as gravure and flexographic printing.

The inks used were custom formulated / synthesized. Metal contacts were formed using gold nanoparticle-based inks using our previously described nanoparticle process [1]. The average diameter of the nanoparticles was ~1.5nm (Fig. 1), resulting in a sintering temperature of ~120ºC, which is compatible with many low-cost plastics. The gate dielectric used a PVP-based ink as reported by several groups. The semiconductor ink was formulated using a soluble pentacene precursor [2]. Upon annealing at plastic-compatible temperatures (~160ºC), the precursor converts to pentacene, which offers substantially improved performance and air stability over most other printable semiconductors.

The process flow for device fabrication is shown in figure 2. The entire process was performed in a custom inkjet printing system using commercial piezoelectric heads from Microfab, Inc [3]. A commercial PET plastic was used as the substrate. The gate electrode was printed at near-ambient temperatures, ensuring the formation of smooth films. Minimum linewidth using the Microfab head was ~120µm. Next, a PVP gate dielectric was printed and thermally cross-linked, followed by gold source/drain electrodes. Various gate dielectric thicknesses were investigated (Fig. 3). To achieve adequate yield with low gate leakage, it was necessary to use relatively thick gate dielectrics formed from multiple layers (Fig. 4, [4]), resulting in high device operating voltages. This is due to the poor jetting stability of the heads used herein and also due to the use of inks formulated using low-purity solvents and materials. Suitable optimization of the materials and printing processes should allow the use of thinner gate dielectrics, thus resulting in reducing operating voltages. The S/D electrodes were printed at elevated temperatures (~150ºC) to insure instantaneous curing. This enabled precise control of linewidth, enabling the reliable realization of lines separated by gaps as short as 15µm (Fig. 5). Based on the linewidth limitations of the gate electrode, a fully-overlapped gate structure was used, enabling realization of devices with channel lengths as short as 15µm, albeit with large overlap capacitance. This is primarily a limitation of the print-head used for this work; several groups have demonstrated inkjetted features as small as 20µm, so use of a suitable head technology should eliminate this problem. The final steps included the printing and annealing of the semiconductor material. As a control, devices were also fabricated using a substrate-gated architecture using heavily-doped silicon wafers with thermal SiO_2 gate dielectrics and evaporated gold S/D electrodes.

Results and Discussion: Electrical characteristics for devices with W=120µm and L=45µm, 15µm are shown in Figs 6-9. The highest mobility observed was 0.17cm^2/V-s, with a maximum gate field of 2MV/cm (due to the thick gate dielectrics, V_{DD} of 40V-100V was used). On-off ratios of 10^4 were obtained. At similar gate fields, the Si-based devices (Figs 10) showed similar mobilities. Interestingly, the silicon devices appeared to have substantially worse S/D contacts, for unknown reasons. To study the electrostatics of these devices, the effect of gate dielectric thickness on device performance was studied. In general, while thinner dielectrics were found to improve on-current and reduce operating voltage, defects in the thinner dielectrics were found to dramatically increase gate leakage, resulting in a reduction in on-off ratio with decreasing $t_{dielectric}$ (Fig. 11). Optimization of the gate dielectric is therefore a crucial issue in need of further study. Despite the use of a thick dielectric, however, the performance of these devices is remarkable. Printing typically results in relatively rough surface layers; the fact that the mobility of these devices is on par with the silicon controls attests to the robustness of the printing process. The good length scaling of the technology down to the limits of our printing ability also attests to the robustness of this technology; insertion of a higher-resolution inkjet head should enable further improvements. Importantly, the performance of these devices is already at a level that is attractive for some printed display applications; further optimization should finally enable the realization of ultra-low cost printed electronic systems, including flexible displays and consumer tags.

0-7803-8684-1/04/$20.00 ©2004 IEEE

[1] D. Huang, *et al*, Journal of the electrochemical society, Vol. 150, pp. 412, 2003.
[2] S. Volkman, *et al*, Proceedings of the Materials Research Society, Volume 769, H11.7, 2003.
[3] S. Molesa, *et al*, Proceedings of the Materials Research Society, Volume 769, H8.3, 2003.
[4] D. Redinger, *et al*, 2003 IEEE Device Research Conference Conference Digest, pp. 187-188, 2003.

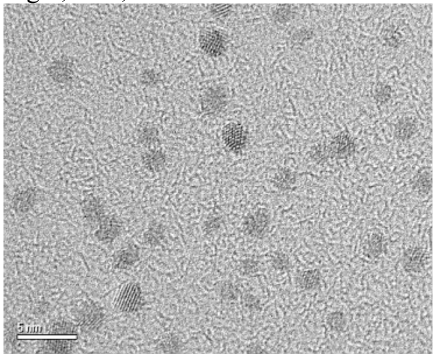

Figure 1: TEM of1.5nm Au particles used for metal contacts.

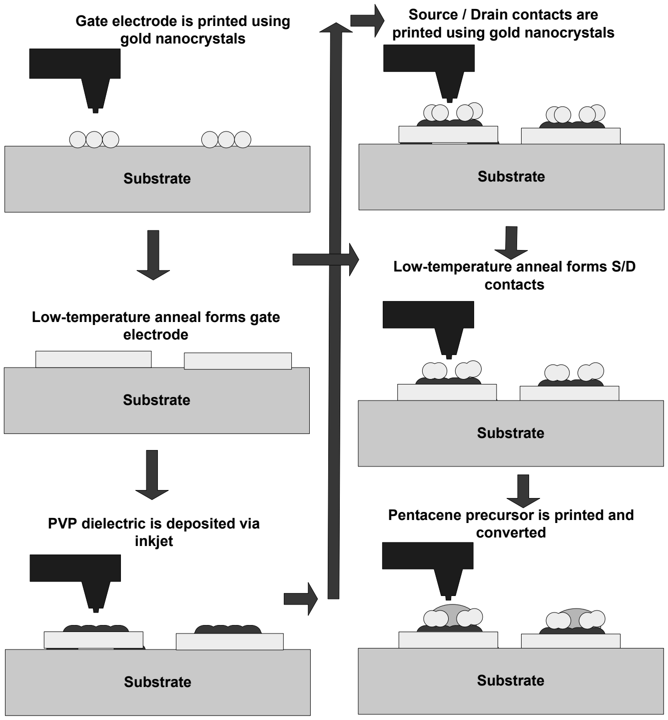

Figure 2: Process flow for formation of printed FETs.

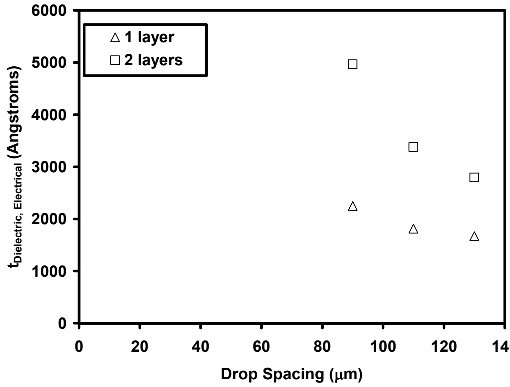

Figure 3: Effect of jetting parameters on thickness of inkjetted dielectric.

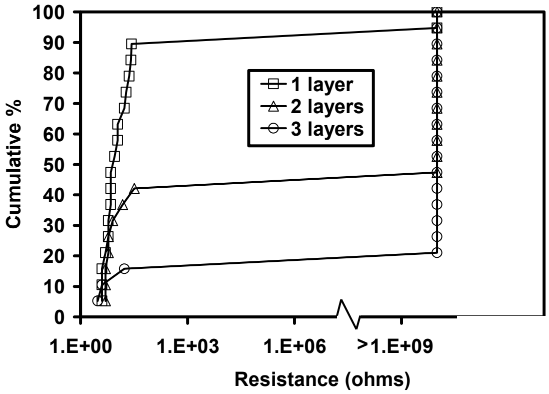

Figure 4: Effect of number of printed dielectric layers on yield due to ink-based defects and jetting instability.

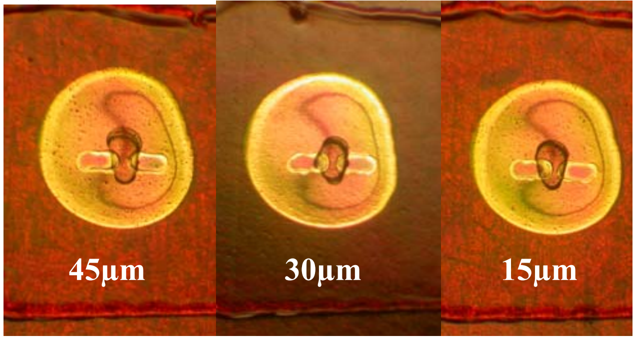

Figure 5: Optical micrographs of various printed FETs.

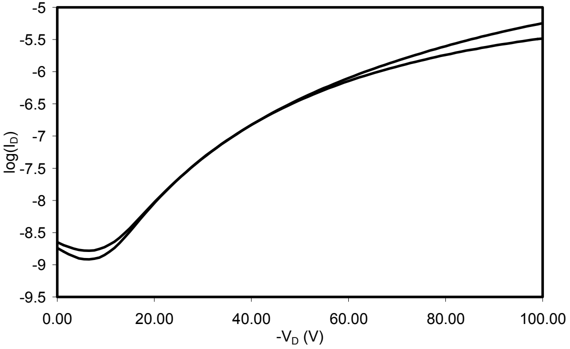

Figure 6: Transfer characteristics for a 120µm/45µm device

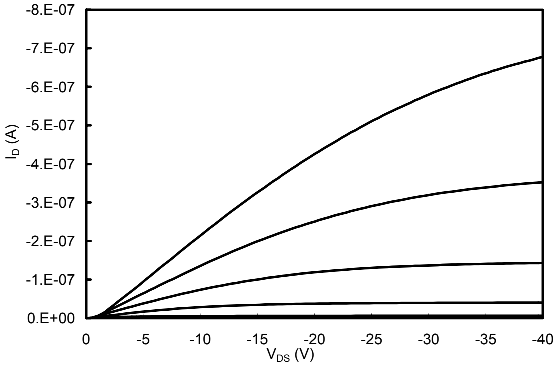

Figure 7: Output characteristics for a 120µm/45µm device (μ ~$0.17cm^2/V$-s)

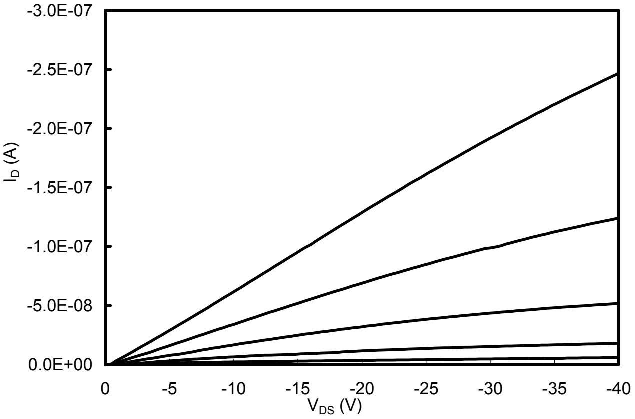

Figure 8: Output characteristics for a 120µm/15µm device (µ ~0.1cm²/V-s)

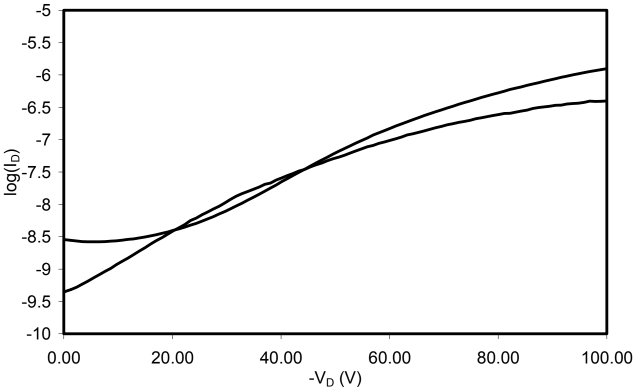

Figure 9: Transfer characteristics for a 100µm/3µm device

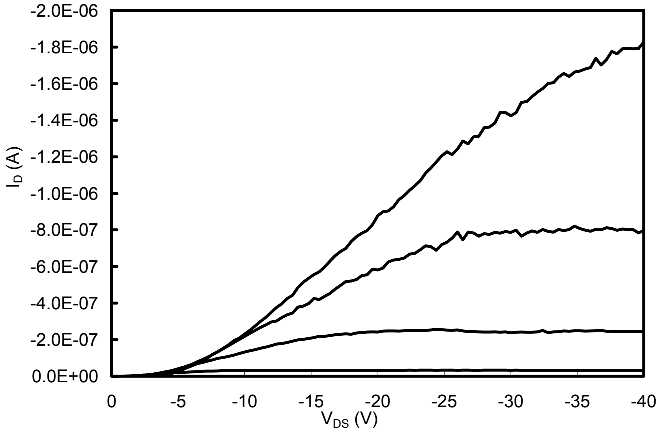

Figure 10: Output Characteristics of OFET on Si/100nm SiO_2 stack, showing similar characteristics to printed FET at equivalent fields.

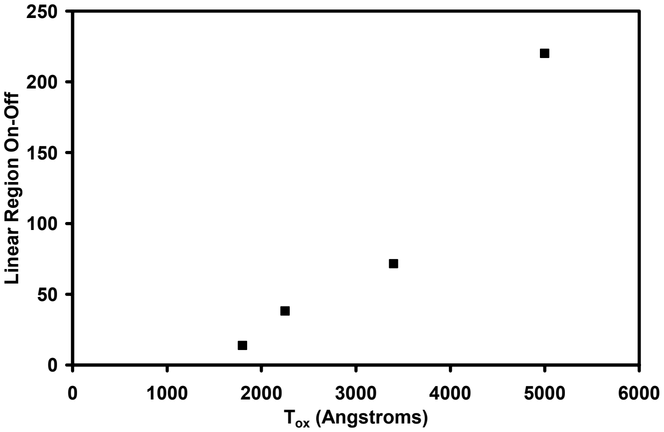

Figure 11: Variation in on-off ratio (in linear regime, at low S/D bias, to ensure uniform gate leakage) with dielectric thickness. Despite increase in drive-current, on-off ratio decreases due to substantially enhanced gate leakage.